WHAT IS CLAIMED IS:

1. A computing system comprising of:
a processor with various power state conditions, wherein the processor performs at a selectable operating mode;
a north-bridge controller;
a south-bridge controller;
a clock;
a power supply; and a
a logic device interfaced to the processor, the north-bridge controller; the south-bridge controller; the clock; and the power supply; whereby the logic device asserts a transition to a different operating mode on the processor while the processor is in a deep sleep power state and upon transition back to operating power state the clock provides a frequency and the power supply provides a voltage matched to the different operating mode.

2. The computing system of claim 1 wherein the logic device monitors a reset condition of the processor, waits for reset to be de-asserted and asserts a performance mode transition.

3. The computing system of claim 1 wherein the logic device passes transition signals from the north-bridge controller to the processor, the transition signals placing the processor in a deep sleep power state and asserting a performance mode transition.

4. The computing system of claim 1 wherein the logic device passes transition signals from the north-bridge controller to the processor, the transition signals placing the processor in a deep sleep power state and asserting a performance mode transition.

5. The computing system of claim 1 wherein the logic device asserts the transition during the normal processor power up sequence.

6. The computing system of claim 1 wherein the logic device asserts the transition following the processor first read only memory (ROM) access.

7. The computing system of claim 1 further comprising:
a memory;
a memory controller; and
a power management controller, wherein the logic device interfaces to the memory, the memory controller, and the power management controller, the logic device performs a suspend to random access memory (RAM) transition keeping power on to the memory, the memory controller, and the power management controller and turning power off and resetting the remaining computing system and processor context is stored in memory, whereby the logic device places the processor in a deep sleep state.

8. The computing system of claim 7 further comprising:
a basic input output system (BIOS) that indicates to the logic device that a suspend to RAM transition will occur.

9. The computing system of claim 7, wherein the logic device blocks a reset on the remaining computer system and allows a reset on the processor.

10. The computer system of claim 9 further comprising:
a basic input output system (BIOS) that indicates to the logic device that a suspend to RAM transition will occur.

11. A method of transitioning a processor having various power state conditions wherein the processor operates a selectable operating mode, the method comprising:
passing control signals from a north-bridge controller capable of placing the processor in a deep sleep state and transitioning the processor into a different operating mode.

12. A method of transitioning a processor having various power state conditions wherein the processor operates a selectable operating mode, the method comprising:

passing control signals from a south-bridge controller capable of placing the processor in a deep sleep state and transitioning the processor into a different operating mode.

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13. A method of transitioning a processor having various power state conditions wherein the processor operates a selectable operating mode, the method comprising:

waiting for the processor to reach a reset state;

resetting the processor; and

asserting a performance mode change on the processor.

14. The method of claim 13 wherein asserting a performance mode is during normal processor power up sequence.

15. The method of claim 13 wherein asserting a performance mode is during processor read only memory (ROM) access.